JOURNAL OF THERMOPHYSICS AND HEAT TRANSFER
Vol. 18, No. 2, April–June 2004

Thermal Performance of Silicon-Die/Water-Cooled Heat-Sink Assembly: Experimental Investigation

E. E. Marotta,* M. Ellsworth,† and S. Mazzuca‡
IBM Corporation, Poughkeepsie, New York 12602
and
J. F. Eberth§
Clemson University, Clemson, South Carolina 29634

The heat flow across a high-powered silicon-die and water-cooled heat-sink assembly is a very important thermal challenge in many microelectronic applications. A single silicon thermal-die/water-cooled experimental facility was fabricated, and a successful experimental program was conducted. Heretofore, unpublished experimental thermal resistance data are presented for two commercially important interstitial materials over a pressure range of 103.4–210.4 kPa (15–30 psi). These results were then compared to thermal resistance data for helium gas, which was flowing at the interface between the two contacting solids. The pressure range employed represents actual operating conditions in an important microelectronic application, which involves chip functionality testing such as silicon burn-in and extended run-in functional operations.

Nomenclature

A_a, A_c, A_g	=	apparent, contact, and gap area, m^2
E_i	=	interstitial material Young's modulus, GPa
F	=	applied force, N
f_g	=	correction factor
h_b	=	bulk conductance, $W/m^2 \cdot K$
h_c, h_g, h_j	=	contact, gap, and joint conductance, $W/m^2 \cdot K$
I_g	=	gap integral
k_g	=	gas thermal conductivity, $W/m \cdot K$
k_i	=	interstitial material conductivity, $W/m \cdot K$
M	=	gas parameter, m
P	=	apparent contact pressure, MPa
$\dot{Q}$	=	joint heat transfer rate, W
R_b	=	bulk resistance, K/W
R_c, R_g, R_j	=	contact, gap, and joint resistance, K/W
R_{int}	=	internal thermal resistance, K/W
RC	=	radius of curvature, m
t	=	final thickness, m
t_g	=	gap, gas thickness, m
t_o	=	original thickness, m
Y	=	mean plane separation, m
σ	=	effective joint surface roughness, $\equiv\sqrt{(\sigma_1^2 + \sigma_2^2)}$, m
ΔT_j	=	joint temperature drop, K

Subscripts

a, c, j	=	apparent, contact, and joint
i	=	index number
1, 2	=	surface of solids 1 and 2

Presented as Paper 2003-0161 at the AIAA 41st Aerospace Sciences Meeting, Reno, NV, 6–9 January 2003; received 3 February 2003; revision received 2 July 2003; accepted for publication 3 July 2003.

*Senior Scientist/Engineer; currently Research Associate Professor, Texas A&M University, College Station, TX 77843-3123.
†Senior Technical Staff Member, Thermal Technologies Group, Product Packaging, Power and Cooling.
‡Manager, Thermal Technologies Group, Product Packaging, Power and Cooling.
§Research Graduate Assistant, Automotive Research Laboratory, Department of Mechanical Engineering.

I. Introduction

A. Microelectronic Applications

MANY modern microelectronic and avionic systems have total dissipated power levels that are increasing with every new packaging design. Increases in power levels and densities combined with the market expectation of reduced package sizes lead to heat challenges that, if left unchecked or uncontrolled, can significantly shorten the operating life of the microelectronic components. Although this increased-power/decreased-size scenario has been prevalent for many decades, the industry's ability to make smaller microelectronic components mandates reduced dimensions for cooling components (e.g., heat sink).

Total power level is not the only problem. Heat density at the silicon device level and localized hot spots are a growing problem, too. This is the direct result of denser electronics via greater number of transistors on a silicon die and increased clock frequencies. Localized die hot spots and high heat-flux densities combined with high overall power levels present the greatest challenge for thermal management engineers, especially for aerospace avionics under vacuum environments. These thermal challenges can cause system failure even if exotic cooling techniques are employed, such as water cooling and/or refrigeration, or if more simple equipments are employed (e.g., heat sinks with proper surface area and airflow).

Liquid cooling, typically a water and glycol mixture, overcomes most of the heat removal and transport limitations of air-cooled systems. Smaller heat sink volumes, elimination of audible noise, the ability to move rejected heat away easily from the user area, and significantly increased system reliability are all liquid-cooling characteristics. The problem is that only a few applications currently accept liquid-cooled electronics. The concept of a liquid-cooled PC and high-end mainframe or server has yet to gain general market acceptance. However, as heat fluxes exceed 50 W per square centimeter, the need for phase-change heat transfer or liquid cooling might be the only alternative. This need for enhanced cooling capacity is evident on today's sophisticated burn-in and extended run-in functional tools where total dissipated power levels can range from 150–400 W while maintaining die junction temperature in the range of 100–140°C. These are indeed very challenging cooling requirements, which must be ensured so that device functional and reliability limits can be achieved.

B. Thermal Interface Materials

The joint thermal resistance to heat flow that incorporates the bulk properties of the graphite interstitial layer can be defined[1] as

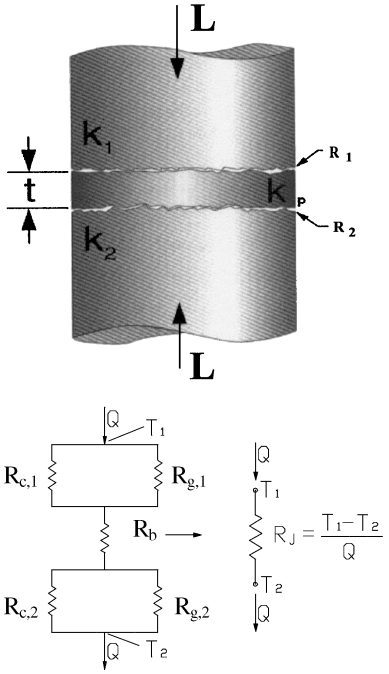

Fig. 1 General diagram of the modeled joint conductance (after Yovanovich et al.[1]).

$$R_j = (1/R_{c,1} + 1/R_{g,1})^{-1} + R_b + (1/R_{c,2} + 1/R_{g,2})^{-1} \quad (1)$$

where $R_{c,1}$, $R_{c,2}$, $R_{g,1}$, and $R_{g,2}$ are the thermal contact resistances, and the thermal gap resistances at each interface, respectively, (see Fig. 1). The thermal joint resistance is defined as the temperature rise across the entire joint divided by the total heat-flow rate. Thus,

$$R_j = \Delta T_j / \dot{Q}_j \quad (2)$$

and, therefore, we can write the following relationship between the thermal joint resistance and the thermal joint conductance (with the apparent area employed) as

$$R_j = 1/h_j A_a \quad (3)$$

The thermal joint resistance can be rewritten in terms of thermal conductance as

$$h_j = 1/[1/(h_{c,1} + h_{g,1}) + 1/h_b + 1/(h_{c,2} + h_{g,2})] \quad (4)$$

Equation (4) is the generalized expression from which the overall joint conductance can be calculated; however, the complexity in computing the individual constituents makes this a very challenging task.

By defining the final thickness in terms of the strain and the bulk thermal conductance with respect to final thickness t and thermal conductivity, a final expression for the joint conductance can be defined as

$$h_b = k_i/t \quad (5)$$

$$t = t_o(1 - P/E_i) \quad (6)$$

$$h_j = [1/(h_{c,1} + h_{g,1}) + t_o(1 - P/E_i)/k_i + 1/(h_{c,2} + h_{g,2})]^{-1} \quad (7)$$

For solid-to-solid interface conductance, Eq. (7) reduces to just the first term; therefore, the bulk conductance and secondary contact and gap conductance terms do not exist.

This investigation was conducted for a particular interstitial material that has shown potential to enhance conductance for ambient environments and, in addition, for heat-sink designs (e.g., variations in heat-sink-to-chip area coverage and heat-sink profile radius of curvature) that might enhance the bare joint conductance. The presence of a gaseous fluid (air or helium in this investigation) at the interface provides a second avenue for heat flow through the interface, as compared to a vacuum; thus, gap conductance considerations must be included in any thermal analysis[2]:

$$h_g = (k_g/\sigma) I_g \quad (8)$$

where

$$I_g = \frac{1}{\sqrt{2\pi}} \int_0^\infty \frac{\exp\left[-(Y/\sigma + t_g/\sigma)^2/2\right]}{t_g/\sigma + M/\sigma} d\left(\frac{t_g}{\sigma}\right) \quad (9)$$

A primary objective of this study was to investigate the effects on thermal joint conductance for a solid-to-solid interface typically found in microelectronic applications (e.g., a silicon die to copper heat sink) caused by the variation of chip power dissipation and interface pressure. Subsequently, the investigation was extended to a solid-to-thermal-interstitial material (TIM) joint. A second objective was to quantify the effect on chip temperatures (e.g., average and maximum values) and chip thermal gradients as a function of chip powers.

C. Outline

Section II, which follows, gives a literature review of the experimental and analytical studies conducted for thermal interface materials, and their effects on thermal joint conductance. Section III presents a schematic of the experimental facility constructed, and its various components, employed for this present investigation. Schematics of the chiller and power assemblies are depicted, which provide both cooling and power to the specially developed thermal device. A LabView program was executed to gather the data created by the extended run-in functional (ERIF) tester and to control the chip power to the heaters. Details of the experimental procedure and parameters employed in the study are also presented. Section IV is devoted to the analysis of the experimental data and their impact on application specific designs/tooling. Summary and conclusions from the research and recommendations for future work are presented in Sec. V.

II. Published Literature

A. Experimental Studies

A review of the literature has revealed that several researchers have conducted analytical and experimental investigations of compliant and elastic thermal interstitial materials.

Miller and Fletcher[3] and Fletcher and Cerza[4] first conducted original work for metal/polymer joints. The authors concluded that thermal conductance values of tested elastomers were lower than the thermal conductance of bare aluminum interfaces. In addition, experimentally gathered data for polyethylene materials in a range of pressures and interface temperatures resolved the effect of carbon filler loading and the effect of increasing temperature.

Ochterbeck et al.[5] investigated the effect on thermal joint conductance of various compounds applied directly onto a polyamide infrastructure. These compounds included several paraffins, diamond-impregnated films, and metallic foils. In all instances, the experimental data showed an increase in thermal joint conductance over bare junctions; however, the paraffin-based compound obtained the greatest improvement or thermal performance increase.

Rauch[6] conducted an experimental study of phase-change interface materials where compounds with and without a supporting system, such as an aluminum foil or a polyamide film, were examined. The nominal melting temperature for these materials was in the range of 51–60°C. The experimentally measured thickness of the phase-change material was observed to decrease in proportion to the applied pressure, and depending on phase change material's (PCM's) viscosity and surface geometric profiles of the contacting surfaces achieved a minimum value. As a corollary observation, the corresponding joint resistance decreased as the time-dependent thickness decreased.

Marotta and Fletcher[7] investigated the thermal conductance of several commercially important polymer materials. Within the range

of apparent interface pressure, the thermal conductance values indicated independence at moderate to high loading. For several thermoplastic polymers, an increase in thermal joint conductance was measured at the higher apparent pressures, which was attributed to material deflection.

An experimental investigation by Mirmira et al.[8] revealed that the thermal joint conductance of several commercially available elastomeric materials became less dependent on apparent interface pressure. These values occurred as the interface loading increased significantly, with the bulk conductance becoming predominant at the high-pressure range (1000–500 kPa). This work was later summarized by Marotta and Han.[9] In addition, for some filled silicone elastomeric materials, such as silver-coated copper powders and silver flakes, thermal conductance values indicated mostly independence on pressure and mean interface temperature as a result of an increase rigidity from the powders and flakes incorporated within its structure.

B. Analytical Modeling

Fuller and Marotta[10] developed an analytical model for the prediction of thermal joint conductance for both thermoplastic and elastomeric polymers placed between metallic solids. The assumptions included nominally flat contacting surfaces, uniform pressure distribution at the interface, elastic deformation of the polymer layer and asperities, and a vacuum environment. Figure 2 shows the results of their analytical and experimental investigation [e.g., Eq. (7) was employed with the gap conductance, $h_g = 0$].

Savija et al.[11] conducted a comprehensive review of analytical and empirical models for calculating the thermal conductance across mechanically formed joints. The paper gave an account of the modeling procedure for a range of contacting interfaces in which the surfaces can be uncoated or bare as well as interfacial surfaces augmented with such materials as greases, films, coatings, polymeric materials, and metallic foils.

Savija et al.[12] presented thermal joint conductance and resistance models for grease-filled joints formed by conforming rough surfaces under light contact pressures. Their proposed models were compared against published greases data presented by Prasher et al.[13] The models and experimental data were found to be in good agreement over a wide range of joint parameter, which was defined as the ratio of effective interface roughness and the thermal conductivity of the gap interstitial material.

Prasher[14] also reported results for specific resistance for two-phase change materials whose thermal conductivity was stated as $k_i = 0.2$ and $0.7\ \mathrm{W/m \cdot K}$, respectively. These results were a result of an experimental investigation to examine the effect of thermal conductivity of grease and phase-change materials and surface roughness on the joint resistance at one contact pressure. It was assumed for phase-change materials that a support structure did not exist and that they behaved like thermal greases.

Marotta et al.[15] provided information on the thermal joint conductance of an important interstitial material employed in microelectronic components. An experimental investigation was conducted for flexible graphite, and then the experimental data were compared to an analytical model developed for elastic layers [Eqs. (5–9)]. The model and data were found to be in good agreement over the pressure range conducted within their investigation. The authors proposed that the model could be used to predict the lower bound on the joint conductance for this class of materials. Figure 3 shows the results of their study for nominally flat, rough surfaces and ambient gap conditions.

III. Experimental Program

A. Experimental Facilities

The purpose of the ERIF tester was to determine the heat-transfer characteristics of various heat sinks and an interface material subjected to a range of heat loads and interface pressures. In addition, the tester needed to provide a controlled environment where heat sinks and interface material could easily be interchanged. The tester consists of multiple parts, which includes the chilled-water subassembly, power subassembly, helium subassembly, pressure-sensing subassembly, and data-gathering subassembly (see Fig. 4).

The chilled-water subassembly provides a mixture of glycol/water coolant at a temperature of 20°C to the heat sink. The chilled-water flow subassembly consisted of a positive displacement chiller, turbine flowmeter, differential pressure transducer, bypass valve, water-temperature sensors, and the tygon tubing and fittings required to connect them in a loop, as shown by Fig. 5.

The power subassembly provided a known quantity of heat load at the chip level to simulate actual microprocessor conditions. It

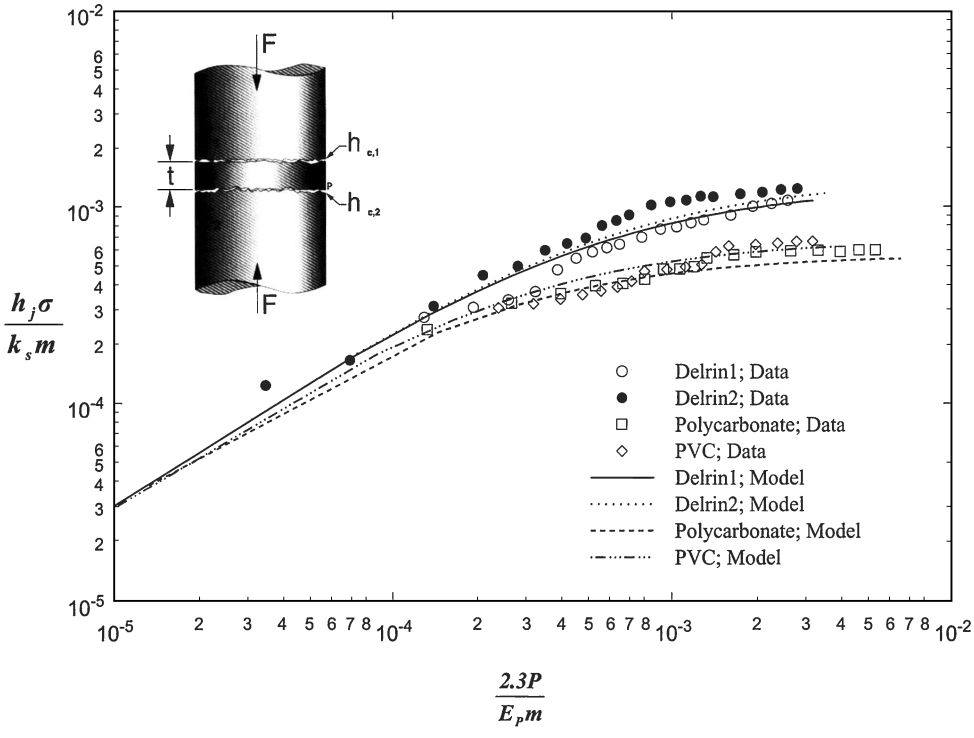

Fig. 2 Dimensionless thermal conductance as a function of dimensionless pressure.[10]

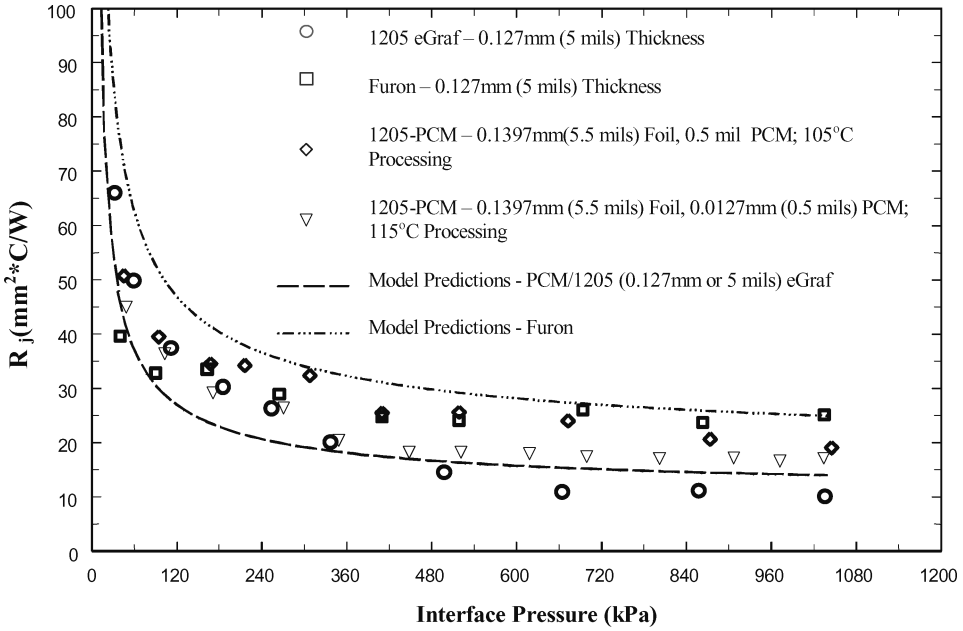

Fig. 3 Thermal joint resistance as a function of apparent interface pressure for phase-change paraffin compound and another commercial graphite material.[15]

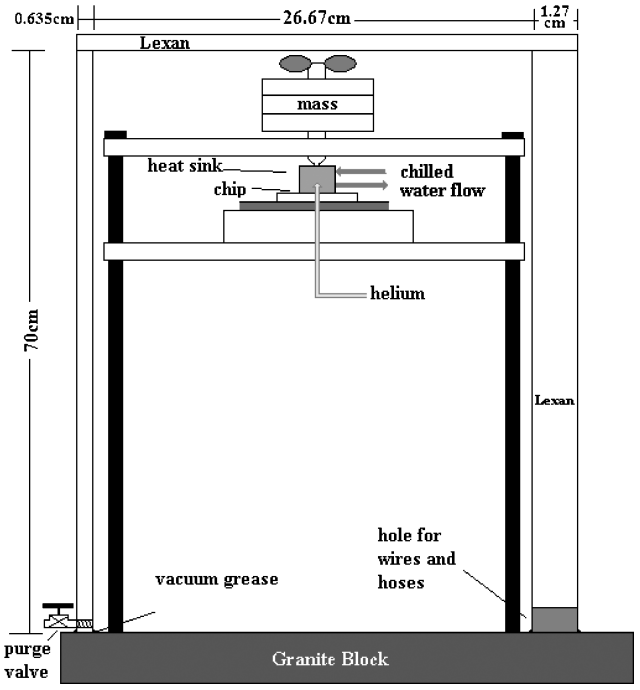

Fig. 4 Schematic of experimental facility.

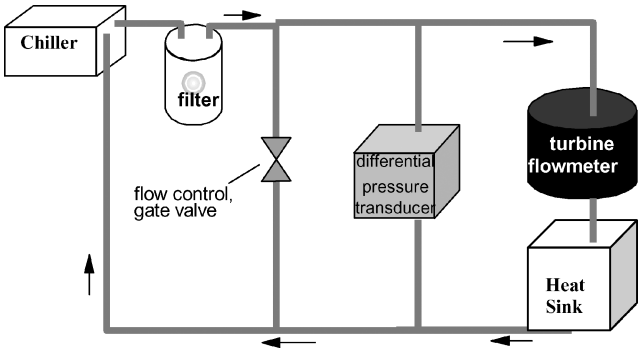

Fig. 5 Schematic of chiller assembly.

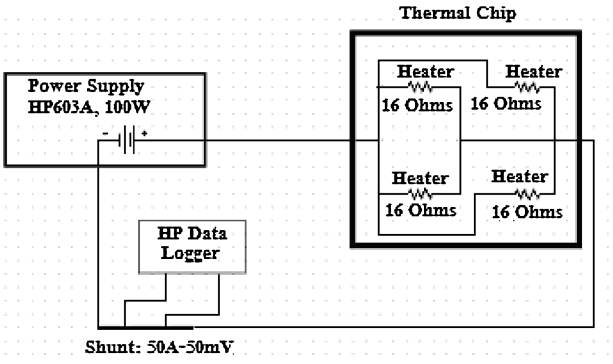

Fig. 6 Schematic of power assembly.

must allow for 0–350 W of power in increments of at least 25 W. The power subassembly consisted of an HP 6030A power supply, shunt, four resistance heaters connected in parallel, and all of the wiring (see Fig. 6).

During bare interface testing conditions, the silicon die was engulfed with helium to allow for enhanced thermal performance at the die/heat-sink interface throughout testing. A large helium tank, with pressure regulator, was connected to a flowmeter and then to the heat sink using tygon tubing.

The helium gas was directed at the die/heat-sink interface through a fitting in the heat sink. An enclosure surrounded the entire ERIF assembly, which aided in the conservation of helium. The helium chamber consists of a Lexan shell and a purge valve to exhaust entrapped air.

A specified load was applied to the top of the chip/heat-sink assembly in order to create a constant uniform pressure at the interface and to maintain the heat sink in place during testing. The pressure subassembly consists of an alignment tower with both a coarse screw alignment adjuster on the chip bracket and a fine screw plunger adjuster at the heat sink. The tower has a threaded rod passing through, which supports weights that transmit a force to dimples located at the top of the heat sink.

A LabView program was executed to gather the data created by the ERIF tester and to control the chip power to the heaters. The subassembly consists of the program, the power supply, the data logger, and connecting cables. The data logger directly reads the chip

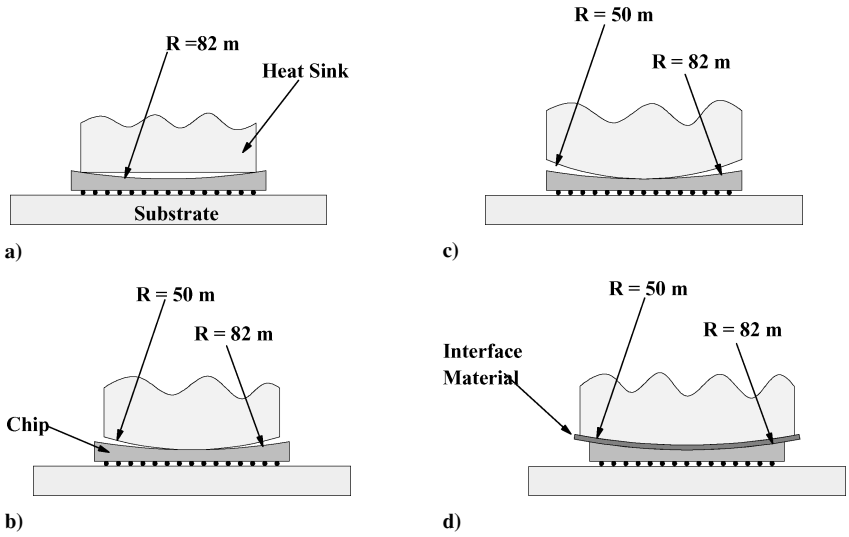

Fig. 7 Chip/heat-sink surface profile configurations.

temperatures from thermal resistors located at strategic points via a four-point probe technique. Seven thermal resistors are read every two minutes to determine steady-state conditions. In addition, inlet and outlet coolant temperatures were gathered as well differential pressure for determining coolant flow rates.

B. Experimental Procedure

Glycol/water inlet and outlet lines were connected to the desired heat sink. All lines were tightly secured to prevent the possibility of fluid damage. When required, a helium gas line was attached to the heat sink via a small hose. Two thermocouples were affixed to the heat sink; one to the side of the pedestal, and the second attached at the helium outlet, located at the center of the heat sink. The thermocouples were then routed to the data logger.

The heat sinks were aligned onto the chip using plunger-type set screws allowing for 0.49 mm of clearance between the heat sink and chip bracket. A force was applied to the heat sink by placing weights onto the top of a long threaded shaft that rested into a dimple located on top of the heat sink. The shaft/weight assembly was fixed, but the entire die assembly was permitted to float during alignment. Set screws, however, prevented the die/heat sink assembly from floating during testing. The force applied was either 5 or 10 kg during each trial. The area of the chip was approximately 393.5 mm^2 so that the pressure was 125.0 kPa or 250.0 kPa. If desired, the force could be applied to the center or to an off-center location using dimples located in each corner of the heat sink.

During the experimental study, not every test employed the use of helium, but most experimental trials did; therefore, a helium chamber engulfed the entire assembly to minimize helium escape into the surrounding room. A constant flow of 14.16 l/min of helium was desired.

The coolant chiller was turned on and allowed to stabilize to 20°C. Adjustments to the chilled coolant bypass valve allowed approximately 1 to 1.2 l/min of flow through the heat sink. A PC-based program forced the experimental test to run for 3 h to achieve steady-state conditions, and then the temperature data were collected.

C. Experimental Parameters

The single-chip ERIF tester was designed in such a way that many different heat-sink configurations and interface materials could be tested while other parameters were held constant. The heat-sink surface had dimensional parameters as follows: 1) 18.5 × 18.5 mm w/flat pedestal, 2) 18.5 × 18.5 mm w/50-m radius of curvature, 3) 19 × 20 mm w/50-m radius of curvature, and 4) 22 × 23 mm with a 50-m radius of curvature.

Each heat sink was first tested without interface material present between the heat sink and the die to obtain bare joint thermal resistance data. Then a flexible graphite material was employed as an interface material for one heat-sink configuration, which showed the overall best reduction in thermal resistance from each configuration. In addition, an 18.5 × 18.5 mm heat sink with tin coating was also examined.

Figure 7 shows a schematic of each silicon-die/heat-sink assembly with and without TIM with their respective surface profiles.

IV. Discussions and Results

A. Thermal Performance Results

The thermal performance of a TIM, such as eGraf 1200 series flexible graphite material, can only be properly assessed if the thermal performance is measured with and without its presence at the junction between the contacting solid surfaces. (eGraf is a trademark of GrafTech, Inc.) This procedure should help elucidate the influence that the bulk material has on the thermal joint resistance, and this would be especially true if metals such as copper or aluminum are employed in the fabrication of the heat sink, because of their propensity to form thin oxide film. Therefore, the study undertook the task of measuring the internal thermal resistance R_{int} when the silicon die was exposed solely to the copper metallic surface, which was the material of choice for the water-cooled heat sink. Figure 8 shows a schematic of the silicon-die/water-cooled heat-sink assembly, along with the corresponding thermal circuit.

The overall thermal circuit includes the resistance caused by spreading (four discrete heat sources were employed), bulk silicon thermal resistance, the silicon-die/copper heat-sink interface, bulk thermal resistance of the copper pedestal, and the combination of the conductive and convective resistances from the pedestal location to the circulating cooling mixture. However, the present investigation did not attempt to undertake the influence on thermal resistance of the heat-sink assembly itself (e.g., external thermal resistance) because this resistance, because of its intrinsic design, is constant for all test runs.

This external thermal resistance was previously determined to be 0.1°C/W, from pedestal thermocouple location, as shown in Fig. 8, to the circulating glycol/water coolant, and, as such, remained constant for the entire range of parameters employed for this present investigation.

The first series of experimental runs attempted to ascertain the influence on silicon die to pedestal thermal resistance for a flat profile heat sink (18.5 × 18.5 mm apparent area) in contact with a concave silicon die, which was initially enveloped with flowing helium gas at the interface and then with a flexible graphite thermal material present at the contacting interface. The experimental data of average and maximum silicon-die temperatures were plotted as a function of applied power, which ranged from 20–300 W, as shown by Fig. 9. In addition, the corresponding internal thermal resistance

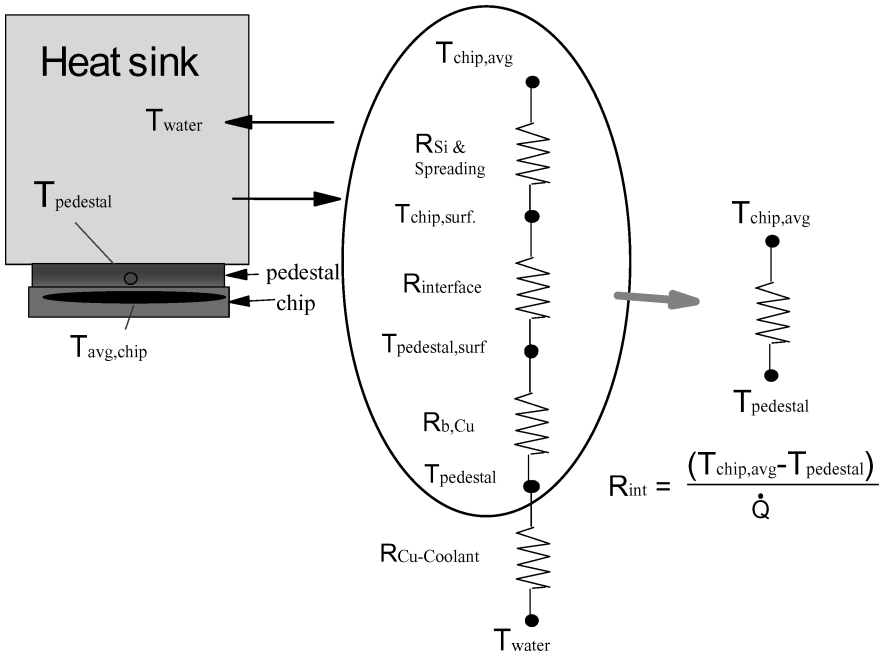

Fig. 8 Thermal resistance circuit for silicon-die/heat-sink assembly.

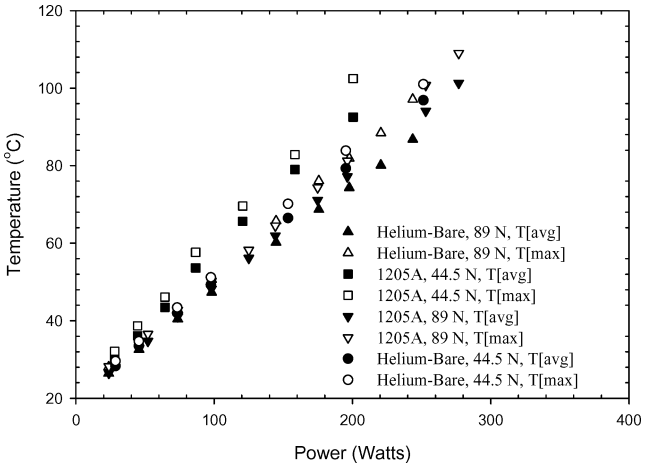

Fig. 9 Silicon-die average and maximum temperatures as a function of applied power (18.5 × 18.5 mm heat sink, flat profile).

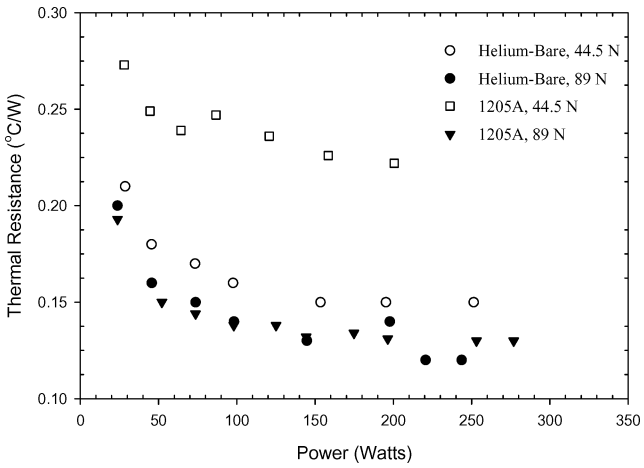

Fig. 10 Thermal resistance from chip to heat-sink pedestal as a function of applied power (18.5 × 18.5 mm heat sink, flat profile).

values were plotted as a function of applied power for both helium gas and flexible graphite material placed at the interface and are shown by Fig. 10.

Figures 9 and 10 clearly indicate that helium gas, which flows at a volumetric rate of roughly 14 l/min, had a significant influence on measured internal thermal resistance R_{int} (see Fig. 8 for an illustration), which is defined as

$$R_{\text{int}} = (T_{\text{avg,chip}} - T_{\text{pedestal}})/\dot{Q} \tag{10}$$

Again, helium gas was directed at the silicon-die/heat-sink interface through a fitting in the heat sink, thus ensuring that gas was always present at the contacting surfaces. The effect on thermal resistance caused by the increased loading force can also be observed; however, its influence was more significant for the flexible graphite material than helium gas. This difference in influence, caused by the greater loading, is a direct result of the compliant nature of the flexible graphite, which the manufacturer claims can be as high as 20% of its original thickness at interface pressures greater than 688.65 kPa (100 psi) and 1.5 to 2% between 103.29 to 206.60 kPa (15 to 30 psi).

The significance of the maximum and average temperature lies in the existence of a highly nonuniform temperature distribution at the chip surface, caused only in part by the spreading resistance of the heat sources but also by the highly nonuniform convective coefficient at the silicon-die/heat-sink contacting surfaces (e.g., at the interface). This will lead to temperature gradients on the silicon-die surface that can range from 30–40°C; this in turn might lead to chip reliability and performance concerns once the final single-chip or multiple-chip modules are assembled and installed into commercial machines. In addition, the average temperatures allow for the calculation of the internal resistance from the silicon-die junction to the copper heat-sink pedestal.

Figures 11 and 12 show experimental data for a silicon die to pedestal thermal resistance for a convex profile heat sink (18.5 × 18.54 mm apparent area) in contact with a concave silicon die, which again was initially enveloped with flowing helium gas at the interface, and then with flexible graphite thermal material. A radius of curvature was diamond turned onto the pedestal surface $RC = 50$ m, which was the desired convex profile requested from the machining vendor, and verified by optical techniques.

Figures 11 and 12 show silicon-die junction temperatures, similar to Figs. 9 and 10, the average and maximum values as well as the calculated internal thermal resistance values as a function of varying applied power. A comparison of the experimental data indicates that the internal resistance was 0.12°C/W and 0.18°C/W, at 10 lbf (44.5 N) for the helium gas and flexible graphite material,

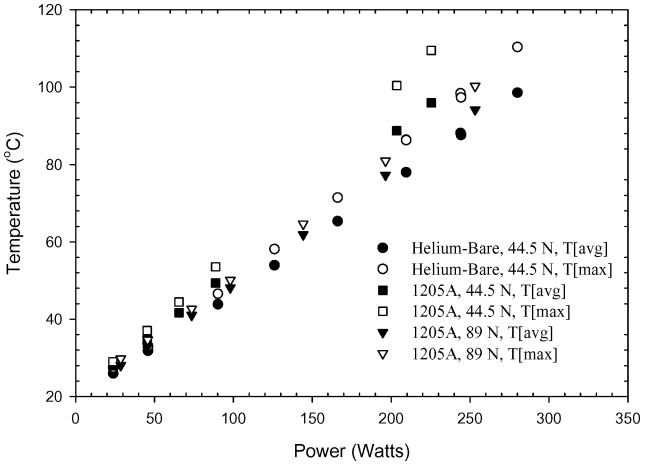

Fig. 11 Silicon-die average and maximum temperatures as a function of applied power (18.5 × 18.5 mm heat sink, 50-m *RC* profile).

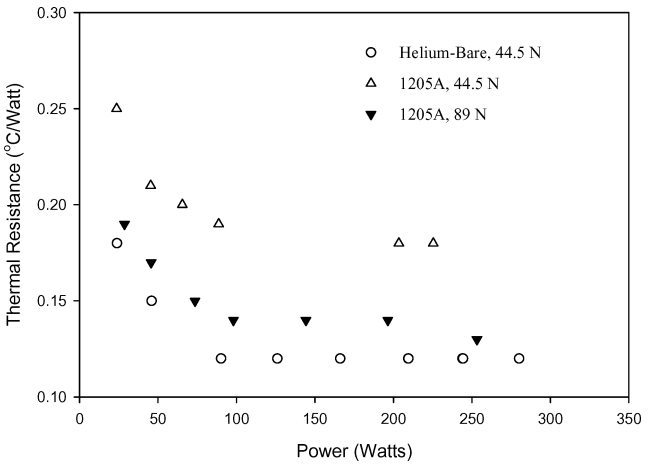

Fig. 12 Thermal resistance from chip to heat-sink pedestal as a function of applied power (18.5 × 18.5 mm heat sink, 50-m *RC* profile).

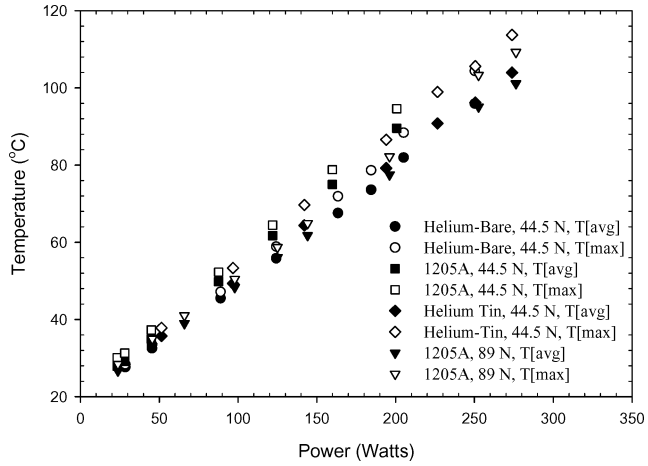

Fig. 13 Silicon-die average and maximum temperatures as a function of applied power (19 × 20 mm heat sink, 50-m *RC* profile).

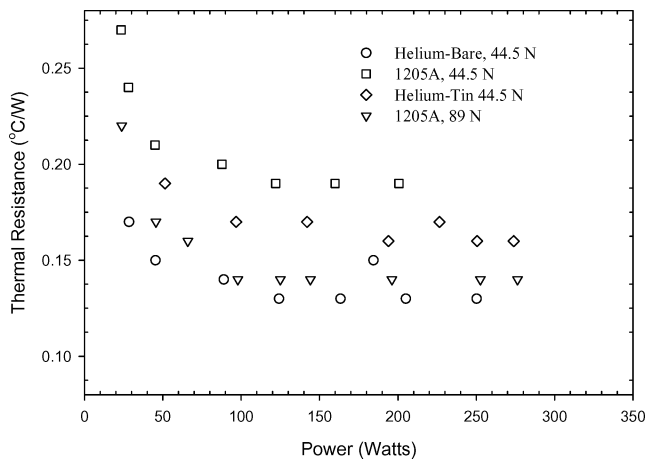

Fig. 14 Thermal resistance from chip to heat-sink pedestal as a function of applied power (19 × 20 mm heat sink, 50-m *RC* profile).

respectively. This indicates a 20 and 22% enhancement, respectively, in thermal performance over the values obtained for the nominally flat 18.5 × 18.5 mm profile heat sink (e.g., 0.15 and 0.23°C/W, respectively). This improvement in thermal performance was a direct result of the minimization of the gap between contacting surfaces, caused by out-of-flatness issues, as depicted in the configurations shown in Figs. 7a and 7b.

The next logical step was to investigate a heat-sink pedestal design, which had similar circumferential dimensions to the silicon die itself, a 19 × 20 mm apparent pedestal area, because this would allow for greater silicon-die surface coverage; and therefore, in theory, greater thermal performance. A similar surface profile value of 50 m for radius of curvature was employed for this set of experimental tests.

Figures 13 and 14 show silicon-die junction temperatures for both the average and maximum values as well as the calculated internal thermal resistance values as a function of varying applied power; however, the heat-sink dimensions are such that the sectional area measured was 19 × 20 mm.

A comparison of internal thermal resistance values for the two heat-sink designs, which contained the 50-m radius of curvature, indicated no improvement because of the increased sectional area. In fact, a slight degradation of the internal resistance values occurred as compared to the smaller pedestal dimensions for both helium and flexible graphite material (e.g., 0.13 and 0.19°C/W, respectively, vs 0.12 and 0.18°C/W, respectively, for the 18.5 × 18.5 mm, 50-m *RC* heat sink). The variations in thermal resistance value are such that they can be deemed equivalent when the experimental uncertainty of the experiments is considered.

Therefore, based on these experimental values, there exists no justification to increase the cross-sectional area of the pedestal and thus attempts to improve thermal performance. In addition, the existence of tin plating at the heat-sink pedestal surface did very little to improve the internal resistance; in fact, its performance was marginally better than the flexible graphite material at a loading of 44.5 N. This result came as a surprise because one would expect better performance as a result of tin's intrinsic mechanical and thermophysical properties. However, one must consider the plating processes employed for the deposition prior to any final judgment on the viability of tin coating. If tin's bulk mechanical and thermophysical properties cannot be replicated when applied as a thin coating, then its use must be questioned for enhancement of contact conductance. At the higher power levels the difference in thermal resistance between the two junctions (i.e., helium-bare to helium-tin) is approximately 0.031°C/W. This value is slightly higher than the uncertainty value of ±0.027°C/W (maximum computed uncertainty value of 17% is taken into account at the lower power levels and smallest temperature drops), and ±0.002°C/W when the lower value of 1% is employed (computed value at the higher power levels and largest temperature drop). Therefore, the difference in thermal resistance between the two junctions is significant and cannot be attributed solely to experimental uncertainty.

The last and final experimental runs involved the use of an oversized pedestal heat-sink design that allowed for an overhang when compared to the silicon die's dimensions. Figure 7d shows a pictorial configuration for this experimental setup. As per Figs. 9–14, the experimental measured die temperatures and internal thermal resistance values were plotted as a function of applied power.

Table 1 Performance summary (helium)

Heat-sink type, mm^2	$R_{int.}$,°C/W	Maximum temperature, °C	Average temperature, °C	Power, W
18.5 × 18.5, flat	0.15	101	97	251
18.5 × 18.5, 50-m *RC*	0.12	110	98	280
19 × 20, 50-m *RC*	0.13	104	96	250
22 × 23, 50-m *RC*	0.09	102	95	293

Table 2 Performance summary[a]

Heat-sink type	$R_{int.}$,°C/W	Maximum temperature, °C	Average temperature, °C	Power, W
18.5 × 18.5, flat	0.13	109	101	277
18.5 × 18.5, 50-m *RC*	0.13	100	94	253
19 × 20, 50-m *RC*	0.14	109	101	276
22 × 23, 50-m *RC*	0.18	106	84	192
22 × 23, 50-m *RC*[b]	0.09	103	91	297

[a]Flexible graphite 1205A–89 N. [b]HiTherm 89 N.

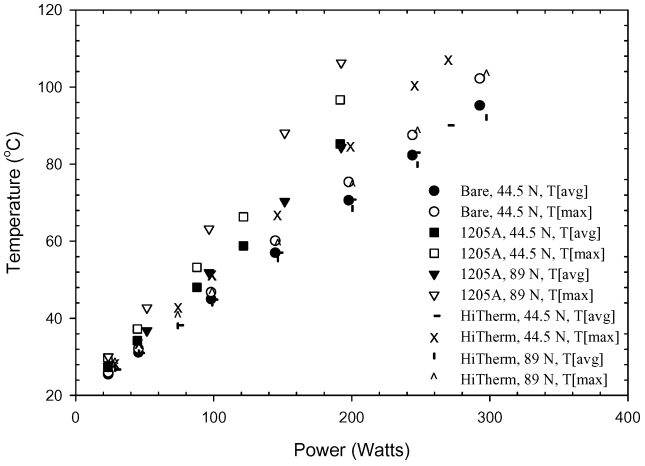

Fig. 15 Silicon-die average and maximum temperatures as a function of applied power (22 × 23 mm heat sink, 50-m *RC* profile).

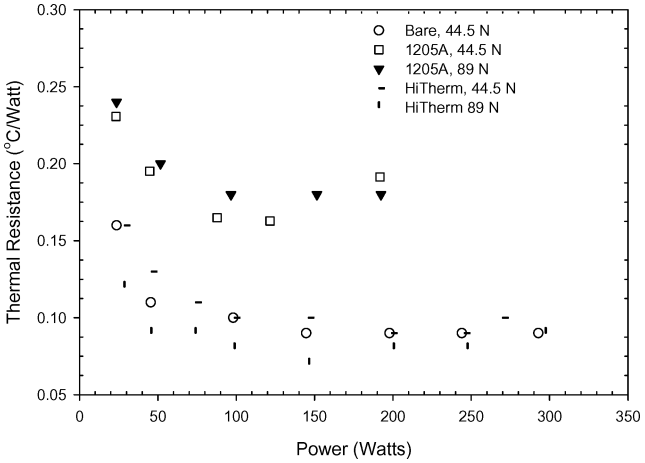

Fig. 16 Thermal resistance from chip to heat-sink pedestal as a function of applied power (22 × 23 mm heat sink, 50-m *RC* profile).

The experimental data gathered included a novel flexible graphite material, which in experimental testing showed a 40% improvement in contact conductance over the 1205 series material with lower applied pressures. Figures 15 and 16 show the experimentally gathered data (average and maximum die temperatures and internal resistance values) as a function of applied power. Similar trends are shown, as Figs. 9–14, with respect to temperatures and internal thermal resistances; however, the HiTherm material showed a significant improvement over its predecessor graphite material.

The experimental data do show increased ability to achieve higher overall power levels, with equivalent die temperatures, over the other heat-sink designs and surface profiles. The much lower internal thermal resistance achieved over the 18.5 × 18.5 mm flat surface profile heat-sink design equally shows this characteristic. A comparison of the experimental data indicates that the internal resistance was 0.09 and 0.17°C/W, respectively, at 44.5 N for the helium gas and flexible graphite material (e.g., 1205 A). This indicates a 40 and 26% enhancement, respectively, in thermal performance over the values obtained for the flat 18.5 × 18.5 mm profile heat sink. The combination of oversized pedestal heat sink and novel flexible graphite material (e.g., HiTherm) showed a 56% improvement in lowering the internal resistance in comparison to the 18.5 × 18.5 flat heat sink. An increase in heat-sink loading from 44.5–89 N further reduced the internal resistance by an additional 10% (e.g., 0.09 vs 0.10°C/W) for the HiTherm graphite material case.

Summary comparisons are presented for internal resistance, temperatures, and highest power level achievable without violation of the allowable maximum chip temperature (e.g., 115°C). Tables 1 and 2 for both helium gas and flexible graphite materials show these summary values. For comparison purposes only, the individual values for the helium gas test runs were for a force loading of 44.5 N because 89 N was not consistently employed or conducted for all tests. Unfortunately, this lack of consistency was caused by time constraints and parameters deemed important to the investigation. The data seem to indicate an equivalency between helium gas at 44.5 N and HiTherm graphite interface material at 89 N, which for cost and manufacturing yield reasons makes this material quite attractive for implementation into the testing procedure.

B. Experimental Uncertainty

In this section, the error analysis of the experimental measurements is presented. Once the accuracy of the measuring instruction is determined, the uncertainty of the calculated internal resistances will be presented.

The overall uncertainty of the experimental results will be calculated using the method described by Moffat.[16] The result of an experiment is determined from a set of measurements, and each measurement can be represented as $X_i \pm \delta X_i$, where δX_i is the uncertainty in the measurement. The effect of each measurement error is determined by

$$\delta R_{X_i} = \frac{\partial R}{\partial X_i}\delta X_i \tag{11}$$

and the overall uncertainty of the results is

$$\delta R = \left[\sum_{1}^{N}\left(\frac{\partial R}{\partial X_i}\delta X_i\right)^2\right]^{0.5} \tag{12}$$

If R is described with the form $R = X_1^a X_2^b \cdots X_N^M$, then the overall uncertainty of the result can be calculated from the set of individual measurement uncertainties:

$$\frac{\delta R}{R} = \left[\left(a \frac{\delta X_1}{X_1} \right)^2 + \left(b \frac{\delta X_2}{X_2} \right)^2 + \cdots \left(M \frac{\delta X_N}{X_N} \right)^2 \right]^{0.5} \quad (13)$$

1. Uncertainty in Temperature Difference (ΔT)

The magnitude of the voltage drop depends on resistor elements embedded into the silicon die and was measured using an Agilent 34970A data logger. A voltage drop of approximately 14–25 mV was measured across each resistor element. The relative uncertainty of the data logger in the 100-mV measurement range as indicated by the instrument's specification was ±0.005%. The magnitude of the constant dc current source supplied by the HP 3497A control unit was 100 μA, which translated into a relative uncertainty of ±0.03% obtained from the manufacturer's performance specification.

With the use of Eq. (12), the relative uncertainty of the calculated resistance $R = V/I$ is the summation of the individual relative uncertainties of the measured voltage and the dc current source supplied. Therefore, the relative uncertainty of the measured resistances is estimated to be ±0.03%. Each resistive element was calibrate to an HP Model 2804A quartz thermometer; the absolute accuracy measurement of the quartz probe within the temperature range of −50–150°C was ±0.02°C with a nominal resolution of 0.001°C. Therefore, the relative uncertainty of the temperature value was ±0.042% at the nominal experimental operating temperature of 47°C. The uncertainty of the measured temperature using type-T thermocouples at the pedestal location was ±0.5°C, which translates into a relative uncertainty of ±1.1% at the nominal operating temperature of 45°C.

The uncertainty in the temperature drop from the silicon-die junction to the heat-sink pedestal location includes the errors of the temperature measurements at both locations, and it was calculated to be ±0.51°C. With a nominal experimental operating temperature of 67°C (mean temperature from the coolant to the maximum allowable chip junction temperature), the relative uncertainty of the temperature drop was ±0.8%. However, the largest calculated relative uncertainty would occur at the highest heat-sink loading and lowest power level setting of 25 W. The mean temperature drop from the chip junction to the circulating coolant at these conditions was 3°C; thus, the maximum relative uncertainty was calculated to be ±17%.

2. Uncertainty in Heat Flow Rate

The relative uncertainty of the heat flow rate through the silicon-die and heat-sink assembly $\dot{Q} = V \cdot I$ is the summation of the individual relative uncertainties of the measured voltage applied and the dc current supplied to the four thermal resistor elements, which were also embedded into the silicon die.

The effective resistance of the four resistances connected in parallel was measured as 4Ω. The power levels dissipated during the experimental runs ranged from 25–300 W. These values translated into a voltage range between 10–35 V, and a current range between 2.5–9.0 amps. The relative uncertainties from the Agilent 6030A power supply, per the vendor's specification, were ±0.08 and ±0.36%, respectively. Therefore, with the use of Eq. (12) the relative uncertainty for the applied power or heat flow rate dissipated from the silicon die becomes ±0.37%.

3. Uncertainty in Thermal Resistance (R_{int})

In our case, the relative uncertainty in the measured internal thermal resistance becomes

$$\delta R/R = [(\delta \Delta T/\Delta T)^2 + (\delta \dot{Q}/\dot{Q})^2]^{0.5} \quad (14)$$

which leads to a relative uncertainty of ±17% for the smallest temperature drop across the silicon-die junction to the pedestal temperature and approximately ±1.0% for the largest temperature drop.

V. Conclusions

The heat flow across a high-powered silicon die and water-cooled heat-sink assembly is a very important thermal challenge in many microelectronic applications. A single silicon thermal-die/water-cooled experimental facility was fabricated, and a successful experimental program was conducted. Experimental thermal resistance data were presented for two commercially important interstitial materials over a pressure range of 103.4–210.4 kPa (15–30 psi). These results were then compared to thermal resistance data for helium gas, which is flowing at the interface between the two contacting solids. The applied loading value employed represents actual operating conditions in an important microelectronic application, which involves chip functionality testing such as silicon burn-in and extended functional run-in operations.

The experimental data indicate that the use of flowing helium gas at the silicon-die/heat-sink assembly performed quite well when a radius of curvature was introduced at the heat-sink surface, which was in contact with the thermal chip. Further, the introduction of an interface thermal material, which becomes more compliant at the higher loading, exhibited results similar to helium gas at the lighter loading level. Thus, the experimental data lend further proof that contour matching, a convex surface profile to concave surface profile, of contacting surfaces improves the contact resistance and thus the internal thermal resistance for these microelectronic applications. In some applications, this enhancement in thermal performance can be quite significant when compared to conventional unengineered contacting surfaces.

Although experimental studies are very important in determining performance limits in microelectronic applications, it has become abundantly clear to the authors that analytical modeling of nonconforming contacting surfaces is paramount to understanding the fundamental physics involved in these complex applications. Promising analytical models developed by prior researchers, such as Yovanovich, Fletcher, Culham, and Marotta, will be investigated for their applicability with thermal interface materials at the contacting surfaces for nonconforming surfaces.

Acknowledgments

The authors acknowledge the support of Graftech, Inc., for supplying the compliant graphite material and its mechanical properties, especially Julian Norley, Brian Ford, and Tom Burkett.

References

[1]Yovanovich, M. M., Culham, J. R., and Teertstra, P., "Calculating Interface Resistance," *Electronic Cooling Magazine*, Vol. 3, No. 2, 1997, pp. 24–29.

[2]Yovanovich, M. M., "New Contact and Gap Conductance Correlations for Conforming Rough Surfaces," AIAA Paper 81-1164, June 1981.

[3]Miller, R. G., and Fletcher, L. S., "Thermal Conductance of Gasket Materials for Spacecraft Joints," AIAA Paper 73-119, Jan. 1973.

[4]Fletcher, L. S., and Cerza, M. R., "Thermal Conductance and Thermal Conductivity of Selected Polyethylene Materials," AIAA Paper 75-187, Jan. 1975.

[5]Ochterbeck, J. M., Fletcher, L. S., and Peterson, G. P., "Evaluation of Thermal Enhancement Films for Electronic Packages," *Proceedings of the 9th International Heat Transfer Conference* 5, Hemisphere, New York, 1990, pp. 445–450.

[6]Rauch, B., "Understanding the Performance Characteristics of Phase-Change Thermal Interface Materials," *Proceedings of ITherm*, Vol. 1, Inst. of Electronics and Electrical Engineers, Piscataway, NJ, 2000, pp. 42–47.

[7]Marotta, E. E., and Fletcher, L. S., "Thermal Contact Conductance of Selected Polymeric Materials," *Journal of Thermophysics and Heat Transfer*, Vol. 10, No. 2, 1996, pp. 334–342.

[8]Mirmira, S. R., Marotta, E. E., and Fletcher, L. S., "Thermal Contact Conductance of Elastomeric Gaskets," *Journal of Thermophysics and Heat Transfer*, Vol. 12, No. 3, 1997, pp. 454–456.

[9]Marotta, E. E., and Han, B., "Thermal Control of Interfaces for Microelectronic Packaging," *Material Society Symposium Proceedings*, Vol. 515, Material Research Society, Warrendale, PA, 1998, pp. 215–225.

[10]Fuller, J. J., and Marotta, E. E., "Thermal Contact Conductance of Metal/Polymer Joints: An Analytical and Experimental Investigation," *Journal of Thermophysics and Heat Transfer*, Vol. 15, No. 2, 2001, pp. 228–238.

[11]Savija, I., Culham, J. R., Yovanovich, M. M., and Marotta, E. E., 2002, "Review of Thermal Conductance Models for Joints Incorporating Enhancement Materials," *Journal of Thermophysics and Heat Transfer*, Vol. 17, No. 1, 2003, pp. 43–52.

[12]Savija, I., Culham, J. R., Yovanovich, M. M., and Marotta, E. E., "Thermal Joint Resistance Models for Conforming Rough Surfaces with Grease Filled Interstitial Gaps," *Journal of Thermophysics and Heat Transfer*, Vol. 17, No. 2, 2003, pp. 278–282.

[13]Prasher, R. S., Simmons, C., and Solbrekken, G., "Thermal Contact Resistance of Phase Change and Grease Type Polymeric Materials," *Proceedings of International Mechanical Engineering Congress and Exposition*, MED-Vol. 11, American Society of Mechanical Engineers, Fairfield, NJ, 2000, pp. 461–466.

[14]Prasher, R. S., "Surface Chemistry and Characteristics Based Model for the Thermal Interface Materials," *Journal of Heat Transfer*, Vol. 123, No. 5, 2001, pp. 969–975.

[15]Marotta, E. E., LaFontant, S., McClafferty, D., Mazzuca, S., and Norley, J., "The Effect of Interface Pressure on Thermal Joint Conductance for Flexible Graphite Materials: Analytical and Experimental Study," *Eighth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems*, IEEE Press, Piscataway, NJ, 2002.

[16]Moffat, R. J., "Uncertainty Analysis," *Electronic Cooling Magazine*, Vol. 5, No. 2, 1999, pp. 32–36.